UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,035	02/18/2004	Jerome M. Eldridge	1303.063US2	2815

21186 7590 10/05/2005

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH
1600 TCF TOWER
121 SOUTH EIGHT STREET
MINNEAPOLIS, MN 55402

EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/781,035	ELDRIDGE ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-71* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4 and 17* is/are allowed.

6)☒ Claim(s) *1-3,5-16 and 18-71* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/06/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's Amendment including Remarks filed 09/06/2005 has been reviewed and placed of record in the file.

Claim Objections

2. Claims 30, 34, 38, 54, 57, 60, 63, and 66, and respective independent claims 31-33, 35-37, 39-41, 55-56, 58-59, 61-62, and 64-65, and 67-68 are objected to because of the following informalities: Claims 30, 34, 38, 54, 57, 60, 63, and 66 each has been argued as having been amended to include the limitation "wherein the intergate insulator barrier height is lower at the floating gate and is higher at the control gate". However, the limitation has not been included in the respective claims. Nevertheless, for examination purposes and for the sake of consistency, the respective claims have been treated as including the limitation.

Appropriate correction is required.

Claim Rejections

3. Applicant's arguments with respect to amended claims 1-3,5-16 and 18-71, filed 09/06/2005, have been considered but they are moot in view of new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. **Claim 1, 2, 11, 15, 48, and 69-70** are rejected under 35 U.S.C. 102(b) as anticipated by Endo U.S. Patent 5,619,051 (the '051 reference, cited in a previous office action).

Referring to **claim 1**, the reference discloses a floating gate transistor, comprising:

a first source/drain region (22 or 24, Fig. 5) and a second source/drain region (24 or 22);

a channel region (no number) located between the first and second source/drain region;

a floating gate (16) operably positioned proximate to and separated from the channel region;

a control gate (20) operably positioned proximate to and separated from the floating gate; and

an intergate insulator (18a) positioned between the floating gate and the control gate, the intergate insulator having a thickness and including a mixture of component oxides ($Ba(Sr)TiO_3$, column 7, lines 1-12) having varied concentrations to provide a composition gradient across the thickness ("a gradient of chemical composition in the thickness direction", paragraph bridging columns 6 and 7) and provide different barrier heights with respect to the floating gate and the control gate (column 7, last paragraph), the component oxides including at least one metal oxide ($Ba(Sr)TiO_3$);

wherein the intergate insulator barrier height is lower at the floating gate and is higher at the control gate (columns 7 and 8, particularly paragraph bridging columns 7 and 8. Specifically, the '051 reference discloses that the forbidden band width of the intergate insulator barrier 18a at the interface with the floating gate 16 is about 3.0eV and that at the interface with control gate 20 is about 3.4 eV (column 7, lines 55+). While it is true that a forbidden band width is not the same as a barrier height, it is known that in the case of non-metal, specifically in the case of an intergate insulator as in the present situation, the barrier height (Fermi level) value lies within the forbidden band width, and this barrier height is dependent upon the characteristics of the materials of the intergate insulator. As the material of the reference' intergate insulator is formed "of a solid solution of two kinds of metal oxides, and the proportions of two metal oxides vary continuously of stepwise from the bottom plane adjacent to the floating gate 16 to the top plane" (column 7, lines 1-8, emphasis added by the

examiner), the Fermi level, or the barrier height, should correspond to the forbidden band. Hence, the forbidden band (value) is narrower (lower), the barrier height is lower, and the forbidden band (value) is wider (higher), the barrier height is higher).

Referring to **claims 11 and 2** and using the reference characters, citations, and interpretations as detailed above for claim 1 where applicable, the '051 reference discloses a device, comprising:

a first source/drain region and a second source/drain region;

a channel region located between the first and second source/drain region;

a polysilicon floating gate (column 3, lines 56-63) operably positioned proximate to and separated from the channel region by an oxide (14);

a control gate operably positioned proximate to and separated from the floating gate; and

an intergate insulator positioned between the floating gate and the control gate, the intergate insulator having a thickness and including a mixture of component metal oxides having varied concentrations to provide a composition gradient across the thickness and provide different barrier heights with respect to the floating gate and the control gate;

wherein the intergate insulator barrier height is lower at the floating gate and is higher at the control gate.

Referring to **claim 15** and using the reference characters, citations, and interpretations as detailed above for claims 1-2 where applicable, the '051 reference discloses a device, comprising:

a first source/drain region and a second source/drain region;

a channel region located between the first and second source/drain region;

a polysilicon floating gate operably positioned proximate to and separated from the channel region by an oxide;

a control gate operably positioned proximate to and separated from the floating gate; and

an intergate insulator positioned between the floating gate and the control gate, the intergate insulator having a thickness and including transition metal oxides ($(Ba(Sr)TiO_3$) having varied concentrations to provide a composition gradient across the thickness and provide asymmetrical tunnel barriers with the floating gate and the control gate;

wherein the intergate insulator barrier height is lower at the floating gate and is higher at the control gate (asymmetrical tunnel barrier intergate insulator 18A, wherein "the dielectric film 18A is formed of a solid solution of two kinds of metal oxides, and the proportions of two metal oxides vary continuously of stepwise from the bottom plane adjacent to the floating gate 16 to the top plane", column 7, lines 1-8, emphasis added by the examiner, and where the "tunnel barrier" property is interpreted to be inherent as the stepwise-graded dielectric layer 18A is a barrier to, for example, electrons tunneling from, for example, from the floating gate to, for example, the control gate; and the characteristic "vary continuously of stepwise from the bottom plane adjacent to the floating gate 16 to the top plane" of the solid solution of the two kinds of metal oxides of the intergate insulator 18A is executed such that there is a difference in tunnel barrier (resulting from the different band gap widths, as detailed above) at an interface with the floating gate and the control gate – hence, asymmetrical – paragraph bridging columns 7 and 8).

Referring to **claim 48** and using the reference characters, citations, and interpretations as detailed above for claims 1-2 and 15 where applicable, the '051 reference discloses a horizontally-oriented device, comprising:

a substrate (10);

a first source/drain region and a second source/drain region located in the substrate, and a channel region located between the first and second source/drain regions;

a floating gate operably positioned over and separated from the channel region;

a control gate operably positioned over and separated from the floating gate; and

an intergate insulator positioned between the floating gate and the control gate, the intergate insulator having a thickness and including a mixture of component oxides having varied concentrations to provide a composition gradient and provide different barrier heights at an interface with the floating gate and at an interface with the control gate, the component oxides including at least one metal oxide;

wherein the intergate insulator barrier height is lower at the floating gate and is higher at the control gate.

Referring to **claims 69 and 70**, the '051 reference discloses a device as claimed and as detailed above for claims 1-2 and 15, but fails to teach the exact method as claimed. However, the limitation is a product-by-process limitation and considered a non-limitation in a device claim.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. **Claims 3,5-10,12-14,16,18-41,49-68 and 71** are rejected under 35 U.S.C. §103(a) as being unpatentable over Endo U.S. Patent 5,619,051 (the '051 reference).

Referring to **claims 22 and 54**, the '051 reference discloses a device as claimed and as detailed above for claims 1-2 and 15, but fails to teach the exact material as claimed. Specifically, the reference discloses a high-dielectric, asymmetrical-tunnel-barrier intergate insulator's material including $Ba(Sr)TiO_3$, an oxide of a transition metal, rather than TiO_2 and ZrO_2 , an oxide of a transition metal and an oxide of another transition metal, as claimed.

However, they are all oxide of a transition metal constituting the high-dielectric, asymmetrical-tunnel-barrier intergate insulator, therefore the change from one material to another material would have been obvious to one or ordinary skill in the art. Referring to the process of claim 54, the limitation is a product-by-process limitation and considered a non-limitation in a device claim.

Referring to **claims 26 and 57**, the '051 reference discloses a device as claimed and as detailed above for claims 1-2 and 15, but fails to teach the exact material as claimed. Specifically, the reference discloses a high-dielectric, asymmetrical-tunnel-barrier intergate insulator's material including $Ba(Sr)TiO_3$, an oxide of a transition metal, rather than TiO_2 and HfO_2 , an oxide of a transition metal and an oxide of another transition metal, as claimed. However, they are all oxide of a transition metal constituting the high-dielectric, asymmetrical-tunnel-barrier intergate insulator, therefore the change from one material to another material would have been obvious to one or ordinary skill in the art. Referring to the process of claim 57, the limitation is a product-by-process limitation and considered a non-limitation in a device claim.

Referring to **claims 30 and 60**, the '051 reference discloses a device as claimed and as detailed above for claims 1-2 and 15, but fails to teach the exact material as claimed. Specifically, the reference discloses a high-dielectric, asymmetrical-tunnel-barrier intergate insulator's material including $Ba(Sr)TiO_3$, an oxide of a transition metal, rather than ZrO_2 and HfO_2 , an oxide of a transition metal and an oxide of another transition metal, as claimed. However, they are all oxide of a transition metal constituting the high-dielectric, asymmetrical-tunnel-barrier intergate insulator, therefore the change from one material to another material

would have been obvious to one or ordinary skill in the art. Referring to the process of claim 60, the limitation is a product-by-process limitation and considered a non-limitation in a device claim.

Referring to **claims 34 and 63**, the '051 reference discloses a device as claimed and as detailed above for claims 1-2 and 15, but fails to teach the exact material as claimed. Specifically, the reference discloses a high-dielectric, asymmetrical-tunnel-barrier intergate insulator's material including $Ba(Sr)TiO_3$, an oxide of a transition metal, rather than TiO_2, ZrO_2 and HfO_2 , an oxide of a transition metal, an oxide of another transition metal, and an oxide of another transition metal, as claimed. However, they are all oxide of a transition metal constituting the high-dielectric, asymmetrical-tunnel-barrier intergate insulator, therefore the change from one material to another material would have been obvious to one or ordinary skill in the art. Referring to the process of claim 63, the limitation is a product-by-process limitation and considered a non-limitation in a device claim.

Referring to **claims 38 and 66** and using the reference characters, citations, and interpretations as detailed above for claims 1-2 and 15 where applicable, the '051 reference discloses a device, comprising:

a first source/drain region and a second source/drain region;

a channel region located between the first and second source/drain region;

a polysilicon floating gate operably positioned proximate to and separated from the channel region by an oxide;

a control gate operably positioned proximate to and separated from the floating gate; and an intergate insulator positioned between the floating gate and the control gate, the intergate

insulator having a thickness and including $Ba(Sr)TiO_3$ to provide a graded mixed oxide insulator, $Ba(Sr)TiO_3$ having varied concentrations across the thickness to provide a composition gradient across the thickness and provide asymmetrical tunnel barriers with the floating gate and the control gate ;

wherein the intergate insulator barrier height is lower at the floating gate and is higher at the control gate.

However, it is clear that the reference does not teach an exact material for the claimed high-dielectric, asymmetrical-tunnel-barrier intergate insulator. Nevertheless, the ability to chose and prepare a material from the known and available materials to form an intended-use product, a high-dielectric, asymmetrical-tunnel-barrier intergate insulator in the instant case, is generally within the ability of a person of ordinary skill in the art therefore would have been obvious.

Referring to the process of **claim 66**, the limitation is a product-by-process limitation and considered a non-limitation in a device claim. Referring to the limitation layers of Al_2O_3 and layers of SiO_2, although the claimed atomic layer deposition in theory and practice is depositing one atomic layer at a time upon the previous one atomic layer– and thus one could call "layers of" – but the final product is a one comprehensible tangible single layer of a high-dielectric, asymmetrical-tunnel-barrier intergate insulator.

Referring to the limitation "wherein a region proximate to the floating gate includes more Al_2O_3 layers and fewer SiO_2 layers than a region proximate to the control gate" of claim 66, which appears to be for the purpose of providing a region proximate to the floating gate with a region of a lower work function than a region proximate to the control gate, the reference teaches

that a region proximate to the floating gate includes more barium titanate and fewer strontium titanate than a region proximate to the control gate, which appears to be also for the purpose of providing a region proximate to the floating gate with a region of a lower work function than a region proximate to the control gate. Hence, again, the difference between the disclosed and the claimed is a choice of the known and available materials tailored for the same purpose, and the ability to chose and prepare a material from the known and available materials to form an intended-use product, a high-dielectric, asymmetrical-tunnel-barrier intergate insulator in the instant case, is generally within the ability of a person of ordinary skill in the art therefore would have been obvious.

Referring to **claims 3, 5-10, 12-14, 16, 18-21, 23-25, 27-29, 31-33, 35-37, 39-41, 55-56, 58-59, 61-62, 64-65, 67-68, and 71,** the '051 patent discloses a non volatile memory cell substantially as claimed and as detailed above for claims 1-2 and 15 and other independent claims including the high-dielectric asymmetrical tunnel barrier intergate insulator 18A including a number of small compositional ranges arranged in a "vary continuously of stepwise" from the bottom surface to the top surface.

The reference further teaches that the floating gate includes a polysilicon floating gate having a metal silicide formed thereon (column 3, lines 56-63) in contact with the asymmetrical low tunnel barrier intergate insulator, and that the control gate includes a metal control gate having a metal oxide layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator (column 4, lines 1-6).

Compared with the claims, the reference discloses a metal silicide instead of the claimed first metal layer for the floating gate, a metal oxide/metal instead of the claimed second

metal/polysilicon for the control gate. However, the differences are deemed to be obvious to one of ordinary skill in the art at the time the invention was made because at least one of the following two reasons: (1) the materials are known and available to the artisan and are provided for the same purpose; (2) both the present invention and the reference fails to show an advantage of one combination of materials to the other, except for the same purpose of providing a high-dielectric, asymmetrical-tunnel-barrier intergate insulator, an intergate insulator barrier height being lower at the floating gate and higher at the control gate.

With respect to the limitation "wherein the metal layer includes a metal layer that has a different work function than the metal layer formed on the floating gate", the limitation appears to be inherent in the reference because: (1) the metal of the metal silicide (functionally equivalent to the claimed first metal) and the metal of the metal oxide (functionally equivalent to the claimed second metal) are different metals, resulting in different work functions; (2) the paragraph bridging columns 7 and 8, as noted above, expressly states that the barrier heights at the two surfaces of the asymmetrical low tunnel barrier intergate insulator, where the metal silicide and the metal oxide are respectively in contact with, ought to be different, leading the artisan to conclude that the work function of the metal silicide (functionally equivalent to the claimed first metal) should be different from the work function of the metal oxide (functionally equivalent to the claimed second metal).

Referring to **claims 49-53**, as detailed above for claims 22, 26, 30, 34, 38, and 42, the ability to chose and prepare a material from the known and available materials to form an intended-use product, a high-dielectric, asymmetrical-tunnel-barrier intergate insulator, an intergate insulator barrier height being lower at the floating gate and higher at the control gate, in

the instant case, is generally within the ability of a person of ordinary skill in the art therefore would have been obvious.

6. **Claims 42-47** are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo U.S. Patent 5,619,051 (the '051 patent) in view of Orlowski et al. U.S. Patent 6,433,382.

Referring to **claim 42**, the '051 patent discloses a non volatile memory cell substantially as claimed and as detailed above for the other independent claims, and including the high-dielectric, asymmetrical-tunnel-barrier intergate insulator 18A and a first source/drain region (22 or 24) and a second source/drain region (24 or 22) separated by a channel region (no number) in a substrate. However, the reference fails to disclose a body region including the channel region and that the body region including the channel region is formed on the first source/drain region. In other words, the reference discloses a "planar" non volatile memory cell instead of a vertical non volatile memory cell as claimed.

Orlowski, in disclosing also a non volatile memory cell including a pair of source/drain regions, a channel region, a floating gate, and a control gate, teaches that vertical non volatile memory cell offers many advantages over a planar non volatile memory cell such as space saving, improved performance, and reduced masking steps (column 14, first paragraph). Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the reference's non volatile memory cell such that it has a vertical configuration. One would have been motivated to make such a change because a vertical non volatile memory cell offers many advantages over a planar non volatile memory cell such as space saving, improved performance, and reduced masking steps, as taught by Orlowski.

Referring to **claims 43-47**, as detailed above for claims 22, 26, 30, 34, 38, and 42, the ability to chose and prepare a material from the known and available materials to form an intended-use product, a high-dielectric, asymmetrical-tunnel-barrier intergate insulator, an intergate insulator barrier height being lower at the floating gate and higher at the control gate in the instant case, is generally within the ability of a person of ordinary skill in the art therefore would have been obvious.

Allowable Subject Matter

7. Claims 4 and 17 are allowable over the prior art of record.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a device having all exclusive limitations as recited in claims 4 and 17, characterized in that the metal layer positioned between the floating gate and the intergate insulator includes a metal corresponding to a metal of a metal oxide, the metal oxide constituting the component oxides that form the intergate insulator that provides a composition gradient across the thickness and that provides different barrier heights with respect to the floating gate and the control gate, wherein the intergate insulator barrier height is lower at the floating gate and is higher at the control gate.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office Action. See MPEP § 706.07(a).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TTH

Tu-Tu Ho
September 21, 2005